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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,809	01/15/2002	Ken Shoemaker	2207/12020	4746

25693 7590 08/29/2005

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,809	SHOEMAKER ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 20 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 9 and 15 rejected under 35 U.S.C. 102(b) as being anticipated by Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors" (hereinafter Eggers).

4. Regarding **claim 1**, Eggers discloses a multi-threading processor, comprising:

a first instruction fetch unit to receive a first thread (page 14, left column: The fetch unit partitions itself among the threads...) and a second instruction fetch unit to receive a second thread (page 14, left column: The fetch unit partitions itself among the threads.);

an execution unit to execute said first thread and said second thread (pages 13 and 14); and

a multi-thread scheduler coupled to said first instruction fetch unit, said second instruction fetch unit, and said execution unit (page 13, left column, see the description of fig.

1c), wherein said multi-thread scheduler is to determine whether the width of said execution unit (page 13, left column, see description of fig. 1c, page 17, right column, last paragraph).

5. Regarding **claim 9,** Eggers discloses a method for scheduling threads in a multi-threading processor, comprising:

determining whether said multi-threading processor is wide enough to execute a first thread and a second thread in parallel (page 12, left column, last paragraph – right column, 1st paragraph: SMT processor exploits both types of thread-level and instruction-level parallelism); and

executing said first thread and said second thread in parallel if said multithreading processor is wide enough to execute the first thread and the second thread in parallel (page 12, left column: SMP processor design which meets simultaneous multithreading because it consumes both thread-level and instruction-level parallelism. Page 13, left column, fig. 1c description: if multiple threads each have low instruction-level parallelism, they can be executed together to compensate).

6. **Claim 15** is rejected on the same ground as stated in claim 9 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors".

9. Regarding **claim 2**, Eggers discloses a SMT system with a processor design to exploit all types of parallelism including consuming both thread-level and instruction-level parallelism and that SMT processors use resources more efficiently (page 12, left column, 2nd paragraph – right column, 1st paragraph). Eggers also discloses that SMT uses instruction-level and thread-level parallelism to substantially increase effective processor utilization and to accelerate both multiprogramming and parallel workloads (page 17, right column, last paragraph). It would have been obvious to one of an ordinary skill in the art, to recognize that the multi-thread scheduler unit in Eggers' system determines whether the execution unit is to execute the first thread and the second thread in parallel depending on the width of the execution unit for effectively utilizing the processor and accelerating both multiprogramming and parallel workloads.

10. Claims 3 – 8, 10 – 14 and 16 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors", as applied to claims 1, 9 and 15 above, in view of Applicant's admitted prior art (hereinafter AAPA).

11. Regarding **claim 3**, Eggers discloses a SMT's system that can perform instruction-level parallelism (page 12, left column, last paragraph). It would have been obvious to one of an

ordinary skill in the art, at the time the invention was made to consider Egger's system an in-order processor because if one thread has high instruction-level parallelism, that parallelism can be satisfied (page 13, left column, 6th paragraph). Furthermore, AAPA discloses that an in-order processor is a well-known architecture in the art (specification page 3, lines 10 – 15).

12. Regarding **claim 4**, as modified Eggers discloses the execution unit executes the first thread and the second thread in parallel (Eggers: page 13, left column, fig. 1c description: if multiple threads each have low instruction-level parallelism, they can be executed together to compensate).

13. Regarding **claim 5**, as modified Eggers discloses the execution unit executes the first thread and the second thread in series (Eggers: page 13, left column, fig. 1c description: if one thread has high instruction-level parallelism, that parallelism can be satisfied).

14. Regarding **claim 6**, as modified Eggers discloses the first thread and the second thread are compiled to have instruction level parallelism (Eggers: page 12, left column, last paragraph).

15. Regarding **claim 7**, as modified Eggers discloses a multi-threading processor comprising:

a first instruction decode unit coupled between the first instruction fetch unit and the multi-thread scheduler (Eggers: page 14, right column, 1st paragraph: the decoder for the first thread instructions); and

a second instruction decode unit coupled between the second instruction fetch unit and the multi-thread scheduler (Eggers: page 14, right column, 1st paragraph: the decoder for the second thread instructions).

16. Regarding **claim 8,** as modified Eggers discloses the execution unit executes only two threads in parallel (Eggers: page 14, left column, 5th - right column, 2nd paragraph: on each cycle, it selects two different threads).

17. Regarding **claim 10,** as modified Eggers discloses a method for scheduling threads comprising executing the first thread and the second thread in series if said multi-threading processor is not wide enough (Eggers: page 13, left column, fig. 1c description).

18. **Claims 11 – 14 and 16 - 20** are rejected on the same ground as stated in claims 3, 6 – 8 and 10 above.

Response to Arguments

19. Applicant's arguments filed 6/8/05 have been fully considered but they are not persuasive for the reasons set forth below.

20. Regarding applicant's argument that Eggers fails to teach or suggest determining whether a multi-threading processor is wide enough to execute a first thread and a second thread in

parallel as recited in claims 1, 9 and 15 (page 11, 3rd and 6th paragraphs), the examiner disagrees for several reasons.

First, claim 1 only recites the limitation the multi-thread scheduler is to determine the width of the execution unit. Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claim subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

Second, Eggers discloses that SMT processor exploits both types of thread-level and instruction-level parallelism and it is designed to meet simultaneous multi-threading because it consumes both thread-level and instruction-level parallelism (page 13, left column, last paragraph – right column, first paragraph). Eggers further discloses "the processor dynamically schedules machine resources among the instructions, providing the greatest chance for the highest hardware utilization. If one thread has a high instruction-level parallelism, that parallelism can be satisfied; if multiple threads each have low instruction-level parallelism, they can be executed together to compensate. In this way, SMT can recover issues slots lots to both horizontal and vertical waste (page 13, left column, see description of fig. 1c). The fact that Eggers' processor exploits both types of thread-level and instruction-level parallelism and schedules to execute multiple threads together, the processor width must have taken into the account to determine that the processor is wide enough in order to schedule and execute those threads together (in parallel). Therefore, the step of determining whether the processor is wide enough to execute both threads in parallel is considered inherent.

21. Regarding applicant's argument with respect to determining whether a multi-threading processor is wide enough to execute a first thread and a second thread in parallel (page 12, 2nd, 3rd paragraphs), the examiner disagrees for the similar reason as stated in the response above.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (page 12, 3rd paragraph), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

22. Regarding applicant's allegation that Eggers teach away from using an in-order processor, the features of claims 3, 11 and 17 (page 12, 4th paragraph), Eggers does not teach away from using the an in-order processor because Eggers discloses processor is able to schedule multiple threads when each have low instruction-level parallelism (page 13, 6th paragraph). By this, it is clearly that Eggers' system can be an in-order processor. Furthermore, applicant's disclosure also states the similar feature as disclosed by Eggers for support with the using of an in-order processor in page 9, lines 3 – 5.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., threads to be processed in order based on the processor, page 12, 4th paragraph) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, claims 3, 11 and 17 rejections are based on the combination of Eggers and AAPA. With respect to applicant's arguments against the references individually (page 12, 4th paragraph), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

23. In response to applicant's argument that the combination Eggers and AAPA are impermissible hindsight and not obvious (page 12, 3rr, 5th paragraphs), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Levy et al. (US 2001/0004755) discloses a system for freeing renaming registers on processors with multiple fetch units.

Shiell et al. (US 5,913,049) discloses a system including multi-stream pipeline unit.

Rivers et al. (US 2002/0174319) discloses a method and apparatus for reducing logic activity in a microprocessor.

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
August 22, 2005

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